Code No. 307/ O

FACULTY OF INFORMATICS

B.E. 4/4 (IT) I-Semester (Old) Examination, May / June 2018

Subject : VLSI Design

Time : 3 hours **Max. Marks : 75**

Note: Answer all questions from Part-A. Answer any FIVE questions from Part-B.

PART – A (25 Marks)

1	Draw the transmission gate structure of 2 input XNOR gate.	3
2	Write about pass characteristics of PFET.	2
3	Obtain the layout of CMOS NOR2 gate.	3
4	List the rules associated with stick diagram representation.	2
5	Draw the basic cells of NOT2, NAND2 using cell based design.	3
6	Write about extension design rule with an example.	2
7	What is refresh operation in DRAM.	2
8	Draw the CPL structure of AND/NAND gate.	3
9	List the tri-state primitives used in verilog.	2
10	Differentiate between initial and always blocks.	3

PART – B (50 Marks)

11	a)	Obtain the CMOS circuits of the following : i) XOR2 gate ii) XNOR2 gate	5
	b)	Explain the drain and transconductance characteristics of NFET.	5
12	a)	Obtain the layouts for series and parallel connected FETS.	5
	b)	Draw the stick diagram representation of 4 i/p AOI gate.	5
13	a)	Draw the RC switch model equivalent circuit for the CMOS inverter and derive the expression for rise and fall times of the inverter.	7
	b)	To drive a load capacitance C_L = 10 PF and to minimize the delay in a cascade of inverters find the number of stages 'N' and scaling factor 'S' of each stage if the input capacitance C_1 = 20fF.	3
14	a)	Discuss the operation of basic IT DRAM cell.	5
	b)	What is pseudo NMOS logic? Obtain the expression for the low output voltage V_{OL} of a CMOS inverter using pseudo NMOS logic.	5
15	a)	Write verilog code for a 4-bit ripple carry adder.	5
	b)	What is cross talk. What are its effects. Write the expression for coupling capacitance C_C between two interconnect lines.	5
16	a)	What is Domino logic? Draw the domino AND and OR gates.	5
	b)	Obtain the expression for time constant of a m-rung ladder structure of a interconnect line interms of line resistance and capacitance.	5
17	Write short notes :		
	a)	Scaling theory	3
	b)	Layout of a Transmission gate	3
	c)	Photolithiography	4

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