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### **FACULTY OF INFORMATICS**

B.E. 3/4 (IT) II-Semester (Supplementary) Examination, January 2013

# Subject : Advanced Computer Architecture (Elective-I)

Time: 3 Hours Max. Marks: 75

Note: Answer all questions of Part - A and answer any five questions from Part-B.

### PART - A (25 Marks)

- 1. Sketch a block diagram to represent the architecture of a vector super computer. (2)
- 2. Illustrate detection of parallelism in a program using Bernstein's conditions. (3)
- 3. List some primitive operations for vector processors and symbolic processors. (2)
- What are the forbidden latencies and the initial collision vector for the reservation table for a four stage pipeline with a clock cycle T = 20 m shown below.

	1	2	3	4	5	6
S1 S2 S3 S4	Χ					X
S2		X		X		
S3			X			
S4				X	X	

- 5. Show how Butterfly network is a restricted subclass of omega networks. (3)
- State and explain briefly any two context switching policies in multithreaded architectures.
- What is the purpose of loop parallelization? Give the two steps to perform loop parallelization.
- parallelization. (3)
  8. Describe parallel flow control. (3)
- 9. List parallel languages for parallel programming. (2)
- 10. How is asynchronous message passing achieved in Linda programming? (2)

#### **PART – B** (5x10=50 Marks)

- 11.(a) Illustrate the following: (5)
  - (i) Data dependence (ii) control dependence (iii) resource dependence
    (b) Draw dependences graph and parallel execution flow using adders for the
    - following instructions labeled  $p_1$ ,  $p_2$ ,  $p_3$ ,  $p_4$  and  $p_5$ . (5)

 $p_1: C = D X E$ 

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 $p_2 : M = G + C$ 

 $p_3 : A = B + C$ 

 $p_4 : C = L + M$ 

 $p_5: F = G \div E$ 

Assume each statement requires one step to execute.

- 12.(a) The performance of memory hierarchy is determined by the 'effective accesstime' at any level in the hierarchy, and depends on the 'nitrations' and 'access frequencies'. Explain.
  - (b) Give a Hierarchy optimization model and explain.
- 13.(a) Explain cache coherence problem. (5)
- 14. Describe in detail the share variable model as a parallel programming
- model. (10)
- 15.(a) Explain synchronous message passing with special reference to Ada. (5)
  - (b) Illustrate Domain decomposition. (5)
- 16. Give SIMD machine model. Write vector instruction types along with examples. (10)
- 17. Write short notes on the following: (10)
  - (a) Conditions for parallelism

(b) Illustrate Snoopy Bus protocol.

- (b) Multithreading Issues and solutions
- (c) Language features for parallelism

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