Code No. 9119

FACULTY OF INFORMATICS

B.E. 3/4 (IT) I – Semester (Main) Examination, Dec. 2014 / Jan. 2015

Subject: Digital Signal Processing

Time: 3 Hours **Max.Marks: 75**

Note: Answer all questions from Part A. Answer any five questions from Part B.

PART – A (25 Marks)

1		Give the three representations of Discrete Time signal with an example.	3
2		Derive the relation between DFT and z-transform.	2
3		The frequency response of a digital filter is $H(e^{jw}) = (0.7 + 0.6 \cos w - 0.9 \cos 2w)e^{-j7.5w}$ Determine the phase delay and group delay.	3
4		What are the desirable characteristics of the frequency response of window function?	2
5		Differentiate between bilinear transformation and impulse invariant transformation.	3
6		Define truncation and rounding used to eliminate lower order bits of the result of an arithmetic operation.	2
7		With a block diagram explain about MAC unit.	3
8		List the major features of programmable digital signal processors.	2
9		Explain about DSP-based biotelemetry receiver system.	3
10		Write short notes on pipelining DSP processor.	2

PART – B (50 Marks)

11	a)	Determine the impulse response and the unit step response of the system described by the difference equation $y(n) = 0.6\, y(n-1) - 0.08\, y(n-2) + x(n)$	6
	b)	Find the linear convolution of x(n) = {1, 2, -1, 2, 3, -2, -3, -1, 1, 1, 2, -1} and h(n) = {1,2} using overlap save method.	4
12	a)	Explain the concept of linear phase FIR filter design using windows. List out the merits and demerits of each window.	6
	b)	Realize the following FIR system with minimum number of multipliers. i) $H(z) = 0.2 + 0.4\, z^{-1} + 0.6\, z^{-2} + 0.4\, z^{-3} + 0.2\, z^{-4}$ ii) $H(z) = (0.3 + \frac{1}{9} z^{-1} + 0.3\, z^{-2})(0.5 - \frac{1}{7} z^{-1} + 0.5\, z^{-2})$	4
13	a)	Explain in detail the Bilinear Transformation method of IIR filter design.	7
	b)	An analog filter has a transfer function $H(s) = \frac{10}{S^2 + 7S + 10}$. Design a digital filter equivalent to this using impulse invariant technique for T = 0.2 sec.	3
14	a)	List out the different registers required to implement circular addressing mode.	3
	b)	Write the steps involved in Pointer updating algorithm for the circular addressing mode.	7
15	a)	Explain in detail the architecture of TMS 320 C54XX DSP processor.	7
	b)	Write short notes on applications of DSP.	3
16	a)	Explain with neat diagrams the computation of 8 point DFT using radix-2 DIT FFT.	7
	b)	Find the circular convolution of the sequences X(n) = {1, 1, 2, 1} Y(n) = {1, 2, 3, 4}	3
17	a)	Explain about the addressing modes of programmable DSP processors.	5
	b)	Draw and explain the structure of 4x4 Braun multiplier.	5

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