Code No. 3134 / O

FACULTY OF ENGINEERING

B.E. 3/4 (ECE) I – Semester (Old) Examination, November 2016

Subject: Digital Integrated Circuits & Applications

Time: 3 Hours **Max.Marks: 75**

Note: Answer all questions from Part A. Answer any five questions from Part B.

PART – A (25 Marks)

1 Differentiate the Digital ICS according to their circuit complexity. 2

2 Define the following and given their topical values in TTL IC's 3

a) V_{IL} b) V_{IH} c) V_{OL} d) V_{OH} e) Noise Margin

3 How many BCD counters are reassured to implement a 3.1/2 digit millimeter display. 2

4 Convert a JK-FF to D-FF. 3

5 Implement the function of (A, B, C) = Σ_n (0, 1, 6, 7) using suitable multi-planer. 2

6 Draw CMOS driver to TTL interface. Why they require an interface explain? 3

7 What are the two major components of disk access time? 3

8 Draw a two input TTL NAND gate with token pole output. Explain the operation of token pole. 3

9 Differentiate between SRAM and DRAMS. 2

10 Draw the interface of TTL to CMOS. 2

PART – B (5x10 = 50 Marks)

11 a) Draw and explain the operation of a TTL 2 input OR Gate. 5
b) Differentiate the features of TTL, family variants 74 L, 74 LS and 74 HC. 5

12 a) Write a short notes on Tri-state logic in TTL. 4
b) Compare the characteristics of TTL, CMOS and ECL. 6

13 a) Realize a 16x1 multiplexer using 4x1 and 2x1 multiplexers. 5
b) Design a 2 bit multiplier using logic gates. 5

14 a) Design a MOD-10 counter using 7490. 6
b) Show how 74490's are cascaded to count 0-9999. 4

15 a) Design 8 K x 8 memory interface using 2 K x 8 PROMS. Draw the diagram showing the circuit. 5
b) What are the advantages of Flash memory over EPROM? Explain different commands used in Flash memory. 5

...2.

16 Design a sequence detector circuit to detect a serial input sequencing of 1010. It should produce an output 'L' whenever the input pattern is detected. 10

Input: 1 0 1 0 1 0 1 0 ...

Output: 0 0 0 1 0 1 0 1 ...

17 Write a short note on any two from the following: 10

a) Saturation logic family

b) Carry look - ahead adder

c) Open drain in CMOS logic family

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