Code No. 3416 / N

FACULTY OF ENGINEERING

B.E. 3/4 (ECE) I – Semester (New) (Main) Examination, November / December 2016

Subject: Computer Organization and Architecture (New)

Time: 3 Hours **Max.Marks: 75**

Note: Answer all questions from Part A. Answer any five questions from Part B.

PART – A (25 Marks)

1 Represent a condition evaluation of a typical expression using RTL with two examples. [2]

2 Specify a sequence of micro-operations that will perform the operation:
   a) IR ← M [PC]
   b) AC ← AC + TR
   c) DR ← DR + AC [3]

3 Show the hardware for implementing Booth's algorithm. [3]

4 Why do we use dividend alignment while performing division operation of binary numbers? [2]

5 Compare Hardwired and Micro programmed control unit. [3]

6 Write the differences between 2 and 3 address instructions. [2]

7 Why does DMA have priority over the CPU when both request a memory a memory transfer? [2]

8 Explain the terms Tag, Index and Block in relation to cache memory. [3]

9 How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 × 16 words? [2]

10 Distinguish between Superscalar and VLIW processors. [3]

PART – B [50 Marks]

11 a) Explain various phases of an instruction cycle in detail. [5]
   b) List the control functions and micro-operations needed for the execution of the following instructions and explain.
      i) ADD
      ii) BSA [5]

12 a) Explain the process of floating point number multiplication with flow chart. [5]
   b) Show the hardware for a 2 bit-by-2 bit array multiplier and explain its working. [5]

13 a) Write the need for addressing modes. Explain various addressing mode supported by a general purpose CPU. [6]
   b) Show how a 9-bit micro-operation field in a microinstruction can be divided into subfields to specify 46 micro-operations. How many micro-operations can be specified in one microinstruction? [4]

14 a) Design a parallel priority interrupt hardware for a system with four interrupt sources. [5]
   b) A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128 × 32.
      i) Formulate all pertinent information required to construct the cache memory
      ii) What is the size of the cache memory? [5]

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15 a) What is Flynn's classification of computers? Explain. [5]
b) List and briefly describe types of Superscalar instruction issue policies. [5]

16 a) Differentiate between Restoring and Non-Restoring division algorithms. [4]
b) Explain instruction pipeline conflicts and their remedies. [6]

17 Write any Two of the following [5 x 2= 10]
a) Isolated Vs Memory mapped I/O.
b) Common bus system.
c) Instruction level parallelism

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