

**FACULTY OF ENGINEERING**

**BE 3/4 (ECE) I-Sem (Old) Examinations, November / December 2012**

**Subject: Computer Organization and Architecture**

**Time: 3 Hours**

**Max. Marks:75**

*Note: Answer all questions from Part-A any five questions From Part-B*

**Part-A (25 Marks)**

1. Draw Flow Chart for a multiplication operation
2. Represent a condition evaluation of a typical expression using RTL with two examples?
3. Differentiate between Hard wired and micro programmed control
4. Write the functions of micro programmed sequences
5. Discuss various types of CPU organizations
6. Write the features of a RISC processor
7. Explain the need for an I/o Interface
8. Draw a chart showing CPU-IOP communication
9. Define association memory & draw a block diagram showing its implementation
10. Write the need for virtual memory concept

**Part-B (50 Marks)**

11. a) Explain the process of floating point number multiplication with a flow chart.  
b) Show the Hardware for a 2 bit-by-2bit array a multiplier & explain its working.
12. a) Explain various phases of an instruction cycles in detail.  
b) Draw the flow chart that explains the complete operations of how an instructions in fetched, decoded & executed in a computer.
13. a) Write the need for addressing modes. Explain various addressing modes supported by a general purpose CPU.  
b) Differentiate between various interrupts?
14. a) Draw the Block diagram of an Asynchronous communication interface and explain its operation in detail.  
b) Explain daisy-chaining process of prioritizing interrupts.
15. Explain various elements of cache design and various mapping techniques used with cache.
16. a) Differentiate between Restoring & non-Restoring division.  
b) Explain one-address, 2-address & 3-address instructions related to CPU organizations.
17. Write a brief note about any two of the following
  - (i) Isolated VS memory mapped I/o.
  - (ii) Memory hierarchy.
  - (iii) Data transfer and manipulation instructions.

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