Code No. 6408/N

FACULTY OF INFORMATICS

B.E. 4/4 (I.T.) I-Semester (New) (Main) Examination, November/December, 2009

Subject : VLSI DESIGN

Time : 3 Hours] **[Max. Marks : 75**

Note : *Answer all questions from* ***Part - A****. Answer* ***any five*** *questions from* ***Part - B****.*

PART - A **(25 Marks)**

1. (a) State Moore's law. 2
   (b) Draw a CMOS logic circuit of a 2-input XOR gate.

2. Consider an n-channel MOSFET with the following characteristic tox = 10nm $\mu_n = 500$ $Cm^2/v\text{-sec}$ $\left(W/L\right) = 8$ $V_{Tn} = 0.75V$. Calculate the device transconductance β_n. 2

3. Draw the CMOS structure for the following : 3
   (a) VIA (b) n MOSFET.

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4. Draw a CMOS logic circuit of a NOR gate and its stick diagram representation. 3

5. Define propagation delay of an inverter. 2

6. An inverter uses FETs with $\beta_n = 2.1\ mA/V^2$ and $\beta_p = 1.8\ mA/V^2$. The threshold voltages are given as $V_{Tn} = 0.6V$ and $V_{Tp} = -0.65V$ and the power supply has a value of $V_{DD} = 5V$. The parasitic FET capacitance at the output node is estimated to be $C_{FET} = 70fF$. Find the mid point voltage. 3

7. Draw the pseudo - nMOs circuit that provide the following logic operation : 3
   (a) $f = \overline{a+b+c}$ (b) $h = \overline{(a+b+c)\cdot x + y\cdot z}$

8. Draw the structure of AND-OR Programmable Logic Array (PLA). 2

9. Write the verilog code for a D flip - flop. 3

10. An interconnect line is made from a material that has a resistivity of $e = 4\ \mu\Omega - cm$. The inter connect is 1200 Å thick ($1\ Å = 10^{-8}cm$). The line has a width of 0.6μm. Calculate the sheet resistance Rs of the line. 2

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PART - B (50 Marks)

11. (a) An n-channel MOSFET has a mobility value of $\mu_n = 560$ cm^2/V-sec and uses a gate oxide with a thickness of tox = 90 Å. The gate voltage is given as $V_G = 2.5$ V. and the threshold voltage is 0.65V. Calculate the value of Cox, k_n' and β_n. Assume the FET has a channel length of 0.25 μm and a channel width of 2 μm. Calculate the current when $v_{DS} = 4$V. 5

(b) Consider the OAI logic function : 5

$$g = \overline{(a+b)\cdot(c+d)\cdot e}$$

Design the CMOS logic gate and explain its function.

12. (a) Draw the layout and stick diagram representation of a NOT and a NOR gate. 5

(b) Explain the latch up problem clearly. How it can be prevented ? 5

13. (a) Derive an expression for the number of stages N required in an inverter cascade to minimize the delay. 5

(b) In an Inverter cascade the load capacitance $C_L = 10$ pF. The input stage is defined with $C_1 = 20$ *fF*. Determine the number of stages required to minimize the delay. 5

14. (a) Draw the general structure of a pseudo nMOS logic and explain. 3

(b) Derive an expression for the low output voltage V_{OL} pseudo n MOS inverter. 3

(c) Draw a tristate inverter circuit and explain its functioning. 4

15. (a) Draw a 4 : 1 MVR using nFET pass transistors and explain. Give verilog code for it. 5

(b) With a suitable diagram explain the function of a 4 bit ripple carry adder. Write the verilog code to construct the same. 5

16. (a) Considering logic gates as basic cells explain the creation of new cell using basic gates. 3

(b) Derive the expressions for the rise time and fall time calculation of a CMOS inverter. 3

(c) Draw the cross section and mask set of n Wells, n^+ region and P^+ region. 4

17. Write notes on the following :

(a) Dynamic RAMs and SRAM arrays. 4

(b) Inter connect modeling. 3

(c) Testing of VLSI circuits. 3

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