Code No. 3302

FACULTY OF INFORMATICS

B.E. 2/4 (IT) First Semester (Suppl.) Examination, June/July 2011

DIGITAL ELECTRONICS AND LOGIC DESIGN

Time : Three Hours] [Maximum Marks : 75

Note :— Answer **ALL** questions from Part A. Answer any **FIVE** questions from Part B.

PART—A (Marks : 25)

1. Define Moore's law. 2
2. Using algebraic manipulation prove that $(x + y)(x + \bar{y}) = x$. 2
3. Give the CMOS realization of a NAND gate with truth table. 3
4. Differentiate between CPLDs and FPGAs. 2
5. What is a prime implicant ? 2
6. Explain Shannon's Expansion theorem. 3
7. What is the difference between latch and flip-flop ? 2
8. Explain Static Hazard with an example. 3
9. Write a VHDL code for 2-to-1 MUX. 3
10. What is the significance of BIST testing ? 3

PART—B (Marks : 50)

11. (a) State and prove DeMorgan laws. 5

    (b) Write a VHDL code for the following functions :

    $f_1 = x_1 \bar{x}_3 + x_2 \bar{x}_3 + \bar{x}_3 \bar{x}_4 + x_1 x_2 + x_1 \bar{x}_4$

    $f_2 = (x_1 + \bar{x}_3)(x_1 + x_2 + \bar{x}_4)(x_2 + \bar{x}_3 + \bar{x}_4)$. 5

12. (a) With a neat block diagram explain FPGA architecture. 5

    (b) Explain any two practical aspects of digital circuit transmission. 5

13. (a) Minimise the following expression using K-maps : 5

    $\Sigma m(5, 6, 9, 10, 12, 13, 14, 15) + d(2, 4)$.

    (b) Illustrate the practical application of multiplexers. 5

14. (a) With timing diagram give the functionality of basic latch. 5

    (b) Design a four-bit ring counter. 5

15. Explain State-Assignment problem with an example. 10

16. Write a VHDL code for an n-bit Shit register with an enable input. 10

17. Write short notes on :—

    (a) Johnson counter 4

    (b) State minimization 3

    (c) PCB testing. 3