Code No. : 6294

FACULTY OF ENGINEERING
B.E. 3/4 (ECE) I Semester (Supplementary) Examination, July 2010
INTEGRATED CIRCUITS AND APPLICATIONS

Time : 3 Hours] [Max. Marks : 75

Note : *Answer* ***all*** *questions from Part A. Answer* ***five*** *questions from Part* ***B.***

PART – A **25**

1. Name the packages available for IC's.
2. Draw the Block schematic of an op. Amp.
3. Distinguish between open collector and tristate outputs.
4. Draw a CMOS transmission gate. What are advantages over an NMOS switch ?
5. A TTL gate is _____ then CMOS gate.

   a) Faster b) Slower c) Bulkier d) Costilier.
6. Multiplexer has:

   a) n input lines and 2^n output lines

   b) n input lines and one out put line

   c) equal input and output lines

   d) none of the above.
7. What are the decimal (equivalents for the code 1001 0110 0011 of this is a

   a) Binary code b) BCD code c) Excess-3 code ?
8. Mention the advantages and disadvantages of shift register counters .
9. Compare serial, parallel and carry look ahead adders.
10. What are the advantages of 2's complement system of arithmetic operations ?

PART – B 50

11. Design an astable multi vibrator circuit. Using 555 timer IC, for a frequency of 1 KHZ with 50% duty cycle and explain its operation with the help of internal functional units of 555 timer IC and wave forms.

12. a) A logic gate has the following specifications :

$V_{iL\,(max)} = 0.6V$ $V_{iH(mm)} = 1.8\ V$

$V_{OL\,(max)} = 0.4\ V$ Volt (min) = 2. 2V

Calculate the two noise margins. If these gates are used in a system, what is the noise margin specification of the system ?

b) Explain the importance and operation of debounced switch.

13. a) Draw the schematic of 4 bit parity generator/checker with control input and give its functional table.

b) Realize a 8 × 1 MUX using logic gates and explain its operation with the help of truth table. How do you realize a 16 × 1 MUX using 8 × 1 MUXes ?

14. a) Give the schematic logic diagram of a BCD Adders/subtractor circuit, and explain its operation with the help of suitable examples.

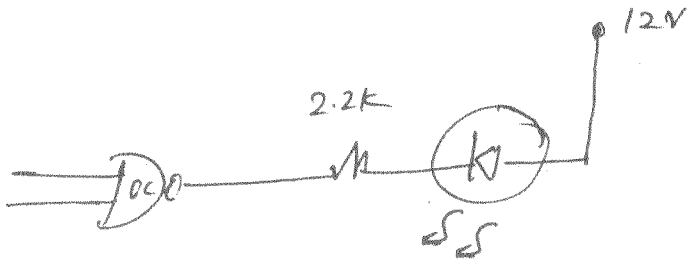
b) Draw the circuit diagram of a 4-bit Right shift and left shift, shift register and explain its operation.

15. a) Show the circuit diagram of a dynamic RAM cell and explain how READ, WRITE and RERESH operations are carried out.

b) Design a ROM system of 1k × 8 bit capacity using 256 × 4 bit ROM devices.

16. a) Briefly explain how 723 can be used to get a +15V power supply. Give all design details.

b) In open collector gate drives an LED as shown below. Calculate the sink current when the LED is on. Assume LED drop = 2 V.



17. a) What is a PLD ? Explain how a PLD can be used to implement 4×4 unsigned multiplier.

b) Compare and contrast a dual slope ADC with a successive approx. ADC.

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