

## FACULTY OF INFORMATICS

B. E. 4/4 (I.T.) I - Semester (Old) Examination, November / December 2009

Subject : VLSI Design

Time : 3 Hours}

{Max. Marks: 75

**Note:** Answer all questions from Part – A. Answer any five questions from Part-B.**PART – A (25 Marks)**

1. Draw the CMOS logic gate for the function  $f = a + b + c$ . (3)
2. Mention six different CMOS layers. (3)
3. Find the device transconductance  $\beta_n$  if the FET has a channel length of  $0.25\mu\text{m}$  and a channel width of  $2\mu\text{m}$ . Given the mobility  $\mu_n = 560 \text{ cm}^2/\text{V-sec}$  and  $C_{ox} = 6.9 \times 10^{-7} \text{ F/cm}^2$ . (3)
4. Consider an nFET that has a channel width  $w = 8\mu\text{m}$ , a channel length of  $L = 0.5\mu\text{m}$  and is made in a process where  $K_n = 180 \mu\text{A/V}^2$ ,  $V_{Tn} = 0.7 \text{ volt}$  and  $V_{DD} = 3.3\text{V}$ . Calculate the resistance  $R_n$ . (3)
5. Write the verilog code for an AoI gate. Draw the corresponding circuit diagram. (3)
6. Write the operation of tristate primitives 'bufifo' and 'notifo', used in Verilog. (2)
7. Draw the logic diagram of a 2x4 decoder. (2)
8. Draw the circuit of a 1T – DRAM cell and its function. (2)
9. Define sheet resistance  $R_s$ . (2)
10. Define Cross talk. (2)

**PART – B (5x10=50 Marks)**

- 11.(a) Explain the different steps involved in a CMOS fabrication. (5)
- (b) Clearly explain the terms "via" and 'action contact'. Draw the diagrams. (5)
- 12.(a) Draw the voltage transfer characteristics of a inverter circuit. Define noise margins for high and low voltages. (5)
- (b) Derive an expression for the midpoint voltage of an inverter circuit. What is a symmetrical inverter ? (5)
- 13.(a) Explain the difficulty of driving a large capacitance load. (5)
- (b) How the delay can be minimized in an inverter cascade and derive an expression for the number of stages for the design ? (5)
- 14.(a) Draw the circuit of a 6T-SRAM cell and explain its function. (5)
- (b) Draw the general structure of a SRAM array. Explain the different blocks and circuits used to achieve the functionality. (5)
- 15.(a) Derive the RC model of an interconnect. (3)
- (b) Explain the principle of operation of a power supply distribution grid. (2)
- (c) What is dynamic switching power ? (5)
- 16 (a) Design a CMOS logic circuit for the OAI expression  

$$h = \overline{(a+b)(a+c)(b+d)}$$
 (5)
- (b) Consider the logic  $g = \overline{a \cdot b \cdot c + d}$ . Design the CMOS logic gate. Explain its operation. Give stick diagram representation (5)
17. Write detailed notes on the following : (5)
- (a) Clocking styles, generation and distribution. (5)
- (b) Ripple carry adder and carry look ahead adders-comparison in terms of delay and hardware. (5)