Code No. 529 / N

FACULTY OF INFORMATICS

B.E. 4/4 (IT) I – Semester (New) (Suppl.) Examination, May / June 2018

Subject: VLSI Design

Time: 3 Hours **Max.Marks: 75**

Note: Answer all questions from Part – A and any five questions from Part – B.

PART – A (25 Marks)

1. What is Moore's law? 2
2. Draw the CMOS logic diagram for a non-inverting buffer. 3
3. List out the advantages of silicon on insulator (SOI) technology over twin tub process. 2
4. What is latch up? How do you prevent latch up problem in CMOS logic? 3
5. How delay is reduced by cascading the inverters? 2
6. Define rise time, fall time and delay time. 3
7. Differentiate between SRAM and DRAM. 2
8. Implement two input AND & NAND gate using complementary pass transistor logic. 3
9. Define cross talk & write the equation for coupling capacitor. 2
10. Write Verilog HDL code for half adder. 3

PART – B (10x5 = 50 Marks)

11. a) Derive current equation of an nMOS transistor in saturation region. 5

    b) Implement the logic function $f = \overline{a.(b+c)}$ using CMOS logic and explain with the help of its truth table. 5

12. a) With the help of neat structure, explain how to make the transistors in series and parallel Connections. 5

    b) Difference between active contact and poly contact. Draw stick diagram of the function

$$f = \overline{A + BC}$$

5

13 a) Draw and explain CMOS process flow. 5

b) With a neat sketch, explain the CMOS inverter switching characteristics. 5

14 a) Draw the block diagram of differential cascade voltage switch logic. Design a two input XOR & XNOR logic gate using above model. 5

b) Explain Read & Write operation of 6T SRAM cell. 5

15 a) Draw & Explain VLSI design flow. 5

b) Implement 4x4 array multiplier & Give one example. 5

16 a) Illustrate the concept of Bubble Pushing. 5

b) Draw CMOS schematic and layout diagram for CMOS inverter. 5

17 a) With the help of neat sketch, explain cell concepts and cell based design. 5

b) Explain about Floor planning and routing. 5

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