Code No. 523 / N

FACULTY OF ENGINEERING

B.E. 4/4 (ECE) I – Semester (New) (Main) Examination, December 2017

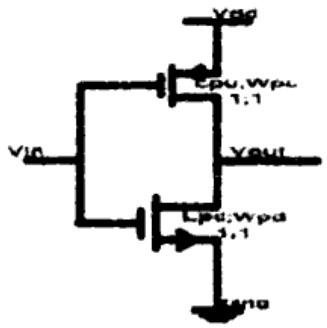
Subject: VLSI Design

Time: 3 Hours **Max.Marks: 75**

Note: Answer all questions from Part A and any five questions from Part B.

PART – A (25 Marks)

1 Draw the I_d Versus V_{ds} curves for an N-channel Enhancement Mode MOSFET ?. (2)
2 Give the expression for channel length Modulation?. (2)
3 Distinguish between SRAM and SRAM. (3)
4 Realize 2:1 Multiplexer using transmission gates. (3)
5 Draw the schematic diagram of BiCMOS inverter. (3)
6 What is crosstalk? How to avoid it?. (2)
7 Draw the schematic diagram of 1 Transistor DRAM cell. (2)
8 Define sheet resistance.? (2)
9 Draw the circuit D-FlipFlop using Transmission Gate?. (3)
10 Calculate the ON Resistance from Vdd to Gnd for the given inverter circuit show in figure. If N- channel sheet resistance is R_{sp} = 2.5 x 10^4 Ω per square? R_{sn} = 10^4 Ω per square



(3)

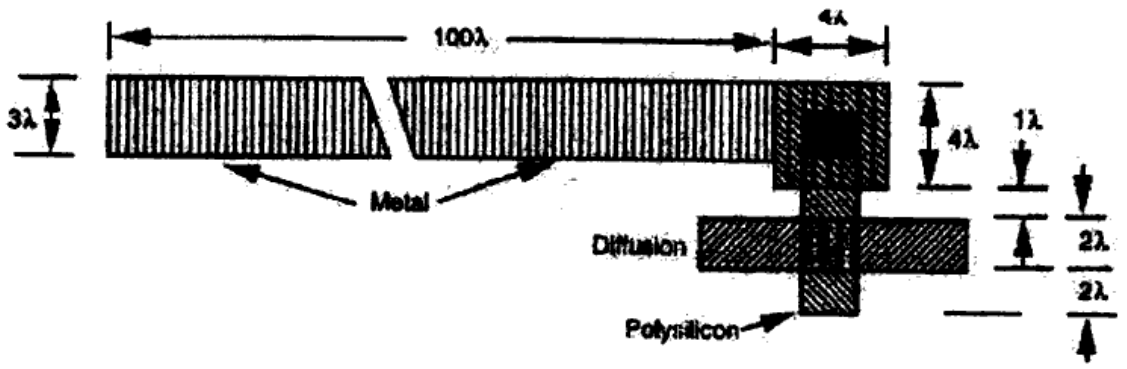
PART – B (50 Marks)

11. a) Derive the drain current expression for n channel enhancement MOSFET operating in Non-Saturation and Saturation Region ? (5)
(b) b) Define the term threshold voltage of MOSFET and explain its significance. (5)

12 12. (a) Draw the stick diagram for the given function (5)
$f = \overline{(A+B)C}$
(b) Determine pull-up to pull-down ratio of an NMOS inverter driven by another NMOS inverter? (5)

13 a) Calculate the gate capacitance value of 5 μm technology with relative in minimum sized transistor with gate to channel capacitance value of 4 x 10-4 pF /μm2 (3)

b) Calculate the Total Capacitance for given layout? 5 μm technology Calculate the total area of capacitance CT for multilayer is shown in figure. Find the CP, Cm, Cg? Given data capacitance across Metal1 to substrate 0.075 pF x 10-4/μm2,Polysilicon to substrate 0.1 pF x 10-4/μm2, Gate capacitance Value 1 Cg

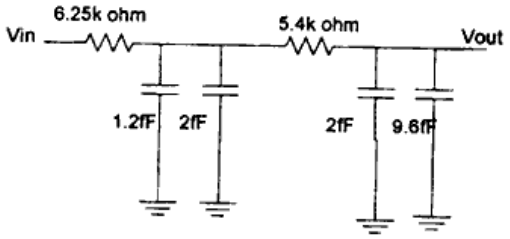


14 (a) Explain & Draw the schematic diagram of 6T SRAM cell? Explain its Read and write operation? (5)

(b) Draw and explain the structure of a Carry select adder. (5)

15.(a) Explain the Interconnect RC delay? Give the Elmore delay calculation? (5)

(b) Explain the Interconnect RC delay? What is propagation delay as calculated by



16 (a) Draw the small signal model for Common Source Amplifier with current mirror and Explain with its characteristics? (5)

b) Draw and Explain the Source degeneration and Wilson Current Mirror? (5)

17. Write short notes on the following

a) Explain the operation of NAND based ROM design? (3)

b) Draw 3T DRAM Cell and explain the write and Read operation? (3)

c) Draw the Layout of NOR Gate? (4)

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