Code No. 3235

FACULTY OF ENGINEERING

B.E. 4/4 (ECE) I-Semester (Main) Examination, November / December 2016

Subject : VLSI Design

Time : 3 hours

Max. Marks : 75

Note: Answer all questions from Part-A. Answer any FIVE questions from Part-B.

PART – A (25 Marks)

1	Write the syntax to declare 4 variables with name 'a' and 4 bits wide.		2
2	Write verilog HDL code for 2 x 1 mux in gate level.		3
3	What is logic synthesis?		2
4	Differentiate between blocking and non-blocking assignments.		3
5	What complications arise due to body effect?		2
6	What are the advantages of CMOS circuits over other MOS circuits?		3
7	Why a good design should follow lambda based design rules?		2
8	What is sheet resistance? Give equation.		3
9	Compare DRAM with SRAM.		2
10	Design 2 input AND gate using 2 x 1 mux.		3

PART – B (50 Marks)

11	a)	What are the features of verilog HDL?	5
	b)	Explain the concept of simulation along with its components.	5
12	a)	Explain compiler directive with examples.	2
	b)	Explain timing control in verilog HDL with examples.	8
13	a)	Derive the equation for IDs taking channel length modulation into account.	6
	b)	Design CMOS EXOR gate.	4
14	a)	Draw stick diagram for 2 input NAND gate.	4
	b)	Explain about BiCMOS inverter.	6
15	a)	What are the draw backs of carry look ahead adder?	2
	b)	Design 4 bit barrel shifter.	8
16	a)	Draw and explain components of verilog module.	5
	b)	Draw 1 bit full adder with 32/28 transistors.	5
17	Write short notes on :		
	a)	Synthesis design flow	5
	b)	Estimation of CMOS inverter delay	5

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