FACULTY OF ENGINEERING

B.E. (ECE) IV – Semester (CBCS) (Main) Examination, May / June 2018

Subject: Pulse, Digital & Integrated Circuits

Time: 3 Hours **Max.Marks: 70**

Note: Answer all questions from Part – A & any five questions from Part – B.

PART – A (10x2 = 20 Marks)

1 Sketch the step response of a High Pass RC circuit.

2 Match the following

a) Attenuator	1. Requires diodes, resistors and capacitors
b) Differentiator	2. Requires diodes and resistors only
c) Clipper	3. Reduces the amplitude of the signal
d) Clamper	4. Low pass RC
	5. High pass RC

3 Compare the performance of series clipper with shunt clipper.

4 With reference to a binary circuit, explain the role of the commutating capacitors.

5 What is hysteresis in a Schmitt Trigger Circuit?

6 Define Fan-out of a logic Gate. What factors determine the Fan-out of a logic Gate?

7 Draw 2 input CMOS NOR gate and write its truth table.

8 Why are MOS ICs especially sensitive to static charge, list its precautions?

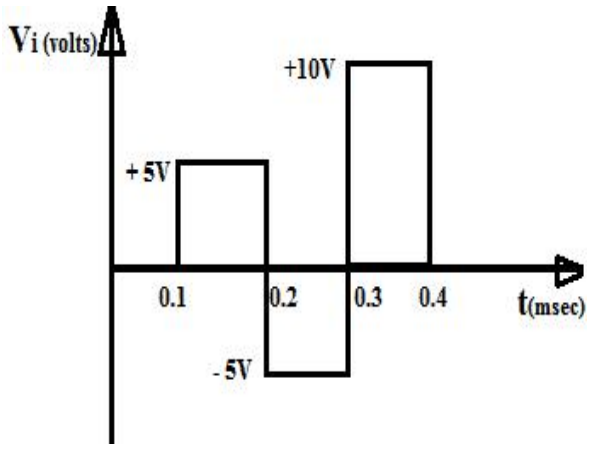
9 Totem pole outputs should not be tied together. Why?

10 What is current sinking and sourcing action in TTL Gate? Show with illustrative diagrams.

PART – B (50 Marks)

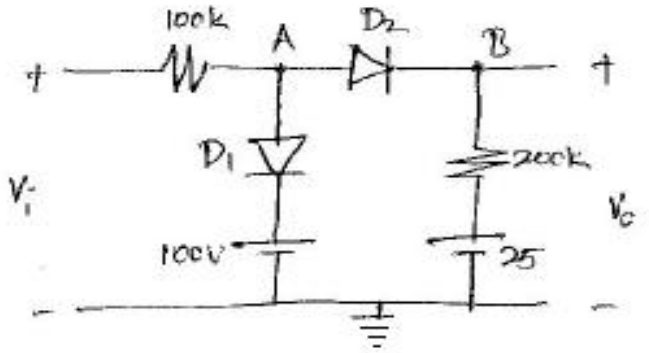
11 a) Show that for any periodic input waveform, the average level of steady state output waveform of RC High Pass circuit is always zero independent of the DC level of the input. 5

b) Assuming the capacitor to be initially uncharged, determine the response of RC Low Pass circuit with a time constant, τ = 0.05 msecs, for the given input waveform in the figure below. 5



12 a) State and Prove the Clamping theorem. 5

b) For the given two level clipper circuit, the input varies linearly from 0V to 150V. Sketch the transfer characteristics to the scale indicating the slopes. 5



13 a) Draw the circuit diagram of a collector coupled astable multi-vibrator and explain it's operation with relevant waveforms at the bases and collectors. Derive the expression for frequency of oscillation. 7

b) In the above collector coupled astable multi-vibrator, find the period of output and the frequency of oscillation if R1 = R2 = 25KΩ and C1 = C2 = 0.2 μ F 3

14 a) Draw and Explain the operation of a 2 input TTL NAND gate using Totem-pole output, for Low output state and High output state with suitable circuit diagrams. State the advantages of totem-pole output circuit. 7

b) A TTL gate is guaranteed to sink 10 mA current with out exceeding an output voltage V_{OL} = 0.4V and to source 1mA current with out dropping below V_{OH} = 2.4V. If I_{IH}= 100uA at 2.4V and I_{IL} = 0.5mA at 0.4V, Calculate the 0 state and 1 state fan out. 3

15 a) How do you interface a TTL gate to a high voltage CMOS gate? Illustrate when each is driving the other. 5

b) What is meant by open-collecter output of TTL gate? What is its utility? Draw and explain the circuit diagram of open-collector output TTL gate. 5

16 a) In a series RLC circuit obtain the transfer function and sketch it's voltage response to a step input. 5

b) Define the three types of errors that occur in time base generators. 5

17 Write short notes on: 10

a) CMOS transmission gate
b) Compensated attenuator.
c) UJT

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