

**FACULTY OF ENGINEERING**

**B.E. 2/4 (ECE) I - Semester (New) (Supplementary) Examination, June 2016**

**Subject : Electronic Devices**

**Time : 3 hours**

**Max. Marks : 75**

**Note: Answer all questions from Part-A. Answer any FIVE questions from Part-B.**

**PART – A (25 Marks)**

- 1 The voltage across the Si diode is 0.7V at 300<sup>0</sup>K and 20mA current flows through it. Calculate reverse saturation current  $I_0$ . ( $V_T = 26\text{mV}$ ). 3
- 2 Distinguish between Zener breakdown and avalanche breakdown mechanism in reverse biased PN junctions. Which break down voltage is higher and why? 2
- 3 A half wave rectifier circuit has a 25V rms sinusoidal AC input and 600 $\Omega$  load resistance. Calculate the  $V_{DC}$ ,  $I_{DC}$  and PIV. 3
- 4 Explain the necessity of bleeder resistor in LC filter. 2
- 5 Define Emitter Efficiency ( $\gamma$ ), Transport Factor ( $\beta^*$ ) and large signal current gain ( $\alpha$ ) of a transistor. 3
- 6 What is an early effect? What are the consequences of it? 3
- 7 Draw the small signal low frequency h-Model of a transistor in BC configuration. 2
- 8 Compare JFET and BJT with various features. 3
- 9 Draw the V-I characteristics of a DIAC. 2
- 10 Classify different types of MOSFETS. 2

**PART – B (50 Marks)**

- 11 a) Derive the expression for diffusion capacitance  $C_D$  in PN junction diode. 5  
b) Draw the energy band diagram of PN junction diode and explain. 5
- 12 a) Find all performance parameters of a centre tapped full wave rectifier circuit. 5  
b) An a.c. supply of 230V is applied to a full-wave rectifier circuit through transformer of turns ratio 5 : 1. Assume the diode is an ideal one. The load resistance is 300 $\Omega$ . Find (a) DC output voltage (b) PIV (c) Maximum, and (d) Average values of power delivered to the load. 5
- 13 a) Describe an experimental set up to obtain the output characteristics of a CE transistor configuration. Indicate and explain the various regions of operation on the output characteristics. <http://www.osmaniaonline.com> 7  
b) Calculate the collector current and emitter current for a transistor with  $\alpha = 0.09$ , and  $I_{CBO} = 100\mu\text{A}$ , when the base current is 50 $\mu\text{A}$ . 3
- 14 a) What is the need for biasing? Define the three stability factors. 3  
b) Consider the self-bias circuit where  $V_{CC} = 22.5$  Volts,  $R_C = 5.6$  K $\Omega$ ,  $R_2 = 10$  K $\Omega$  and  $R_1 = 90$  K $\Omega$ ,  $h_{fe} = 55$ ,  $V_{BE} = 0.6\text{V}$ . the transistor operates in active region. Determine i) Operating point and ii) Stability factor. 7

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- 15 a) Draw the hybrid model for CE amplifier and derive for current gain, input impedance, voltage gain and output admittance. 7  
b) Why N-channel MOSFETS are preferred than P-channel MOSFETS. 3
- 16 a) Explain the construction and working of a N-channel JFET with drain and transfer characteristics. 7  
b) Define  $g_m$ ,  $r_d$  and  $\mu$  of a JFET and derive the expression for  $g_m$ . 3
- 17 Explain short notes on the following : 10  
a) Bias compensation using diode  
b) SCR  
c) CCD

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